REMARKS

Claims 1-20 were pending in this application.

Claims 1-20 have been rejected.

Claims 1, 3-6, 8, 11, 13-16, and 18 have been amended as shown above.

Claims 1-20 remain pending in this application.

Reconsideration and full allowance of Claims 1-20 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,600,345 to Boutaud ("*Boutaud*"). This rejection is respectfully traversed.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

Boutaud recites a clock selection circuit for selecting one of multiple clock signals. (*Abstract*). As shown in Figure 4a, the circuit includes synchronization logic 406, synchronization logic 408, and AND gates 442, 446. (*Col. 7, Lines 35-61; Col. 8, Lines 37-45*). The synchronization logic 406 and synchronization logic 408 produce two enable signals that are input to the AND gates 442, 446 along with two clock signals. (*Col. 7, Lines 50-57*). The AND

gates 442, 446 and an OR gate 440 output one of the two clock signals depending on the enable signals. (*Col. 8, Line 60 – Col. 9, Line 6*).

Claims 1 and 11 have been amended to recite that a first of the "clock control circuits" includes a "first flip-flop," a "second flip-flop coupled in series with the first flip-flop," and an "OR gate having a first input coupled to an output of the first flip-flop and a second input coupled to an output of the second flip-flop." The AND gates 442, 446 of *Boutaud* are relied upon in the Office Action as anticipating the first and second "clock control circuits" recited in Claims 1 and 11. Because the AND gates 442, 446 of *Boutaud* do not include two flip-flops and an OR gate, the AND gates 442, 446 of *Boutaud* cannot anticipate the "first clock control circuit" recited in Claims 1 and 11. Moreover, the OR gate 440 of *Boutaud* does not have two inputs coupled to the outputs of two flip-flops coupled in series. In addition, while Figure 4a of *Boutaud* includes various flip-flops and OR gates, none of the flip-flops and OR gates are arranged as recited in Claims 1 and 11. As a result, *Boutaud* does not anticipate all elements of Claims 1 and 11.

For these reasons, *Boutaud* does not anticipate the Applicant's invention as recited in Claims 1 and 11 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 1-20.

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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